## REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 1-8 and 10-22 remain in the application. Claim 1 has been amended. Claim 9 has been cancelled. Claims 15-22 have been withdrawn.

In item 6 on pages 3-4 of the above-mentioned Office action, claims 1-3, 5, and 9-14 have been rejected as being anticipated by Glenn et al. (US Pat. No. 6,448,506) under 35 U.S.C. § 102(b).

The rejection has been noted and claim 1 has been amended in an effort to even more clearly define the invention of the instant application. Support for the changes is found in original claim 9.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 1 calls for, inter alia:

at least two wiring boards stacked on top of one another and substantially parallel to one another, at least one of said at least two wiring boards having apertures formed therein, said stacked wiring boards including an uppermost wiring board and an undermost wiring board, and at least one of said uppermost wiring board and said undermost wiring board having near-edge electrical contacts without said apertures. (Emphasis added.)

Figs. 5-8 of Glenn et al. show various stacked packages.

However, in each case every layer 70 and/or 72 of the stack
has apertures. Only the motherboard 78 to which the stack is
attached has no apertures. However, the language of claim 1
of the instant application clearly refers to the stack and not
to the motherboard to which it is attached.

In contrast, according to the invention of the instant application, at least one of the uppermost wiring board and the undermost wiring board has near-edge electrical contacts without apertures. This feature of the invention of the instant application is a clear improvement over that of Glenn et al. because it offers the advantage of enabling a range of methods for contacting the stack to further electrical circuits as described on page 6, lines 9-25 of the specification.

Clearly, Glenn et al. do not show "at least two wiring boards stacked on top of one another and substantially parallel to one another, at least one of said at least two wiring boards having apertures formed therein, said stacked wiring boards including an uppermost wiring board and an undermost wiring

board, and at least one of said uppermost wiring board and said undermost wiring board having near-edge electrical contacts without said apertures", as recited in claim 1 of the instant application.

Claim 1 is, therefore, believed to be patentable over Glenn et al. and since claims 2-3, 5 and 10-14 are ultimately dependent on claim 1, they are believed to be patentable as well.

In item 8 on page 4 of the above-mentioned Office action, claim 4 has been rejected as being unpatentable over Glenn et al. in view of Isaak (US Pat. No. 6,180,881) under 35 U.S.C. § 103(a).

As discussed above, claim 1 is believed to be patentable over the art. Since claim 4 is ultimately dependent on claim 1, it is believed to be patentable as well.

In addition, Isaak teaches, as seen for example in Figs. 3-4, s chip stack 10 including chip packages 12 and 14 mounted in a chip carrier 16. The chip carriers are connected electrically via "metallic spheres or balls 24" (see column 6, line 22) which are "mounted in the apertures 22 using conductive epoxy or solder" (see column 6, lines 45-46). Clearly, Isaak does not disclose the subsequent melting of those balls within the

Applic. No.: 10/090,289 Amdt. Dated October 17, 2003 Reply to Office action of July 25, 2003

apertures to form the electrical connections and does not disclose the use of solder balls to act as spacers while building the stack.

In item 9 on page 5 of the above-mentioned Office action, claims 6-8 have been rejected as being unpatentable over Glenn et al. in view of Arakawa et al. (US Pat. No. 6,472,734) under 35 U.S.C. § 103(a).

As discussed above, claim 1 is believed to be patentable over the art. Since claims 6-8 are ultimately dependent on claim 1, they are believed to be patentable as well.

The element referred to by reference number "15" in Fig. 5 of Arakawa et al. is clearly a coating of the whole semiconductor element 13 and is described as such in column 1, line 47:

"Each semiconductor element 13 is sealed with resin 15, such as epoxy resin, so as to cover its top and sides." As described in page 5, lines 7-14, of the specification of the instant application, "the supporting points represent a defined bearing point for the successively following wiring boards of the stack. Even if there are slight differences in the diameter of the solder balls and/or of the apertures in which they come to lie, there is no risk of any direct contact between the wiring board and the semiconductor chip of

Reply to Office action of July 25, 2003

different stacking levels." This is achieved by the plastic buffer 14, as seen in Figs. 2-4, as it is clearly much smaller than the semiconductor chip 2 and acts as a supporting point. This is also described on page 5, lines 16-20. This improvement to the mechanical stability of a stack by the use of a central supporting point is not disclosed by any of the cited references.

In addition, it is noted that the reference Arakawa et al. has a filing date of March 7, 2001 which is later than the priority date March 2, 2001 of the instant application. The reference Arakawa et al. is therefore not available as prior art and the rejection in item 9 on page 5 of this Office action is moot.

Applicant has already filed a Claim for Priority including a certified copy of German application 101 10 203.8 on March 4, 2002. In order to perfect the priority, a certified English translation of the German priority application 101 10 203.8 is enclosed herewith.

In view of the foregoing, reconsideration and allowance of claims 1-8 and 10-14 are solicited.

Applic. No.: 10/090,289

Amdt. Dated October 17, 2003

Reply to Office action of July 25, 2003

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate a telephone call so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made. Please charge any fees which might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

LAURENCE A. GREENBERG REG. NO. 29,308

For Applicant

YHC:cgm

October 17, 2003

Lerner and Greenberg, P.A.

Post Office Box 2480

Hollywood, FL 33022-2480

Tel: (954) 925-1100 Fax: (954) 925-1101